University of Pittsburgh | Informatics and Networked Systems
School of Computing and Information

You are receiving this email because you are enrolled in the MSIS/MST graduate degree programs within the Department of Informatics and Networked Systems at the School of Computing and Information. Each weekly newsletter will feature important updates on career/academic and job opportunities, department and school events, enrollment guidance and upcoming academic deadlines.

Spring Term 2023 Enrollment Appointment Office Hours

Monday: 10am to 11am, available virtually at *https://pitt.zoom.us/j/91954241565*
Tuesday: 2pm to 4pm, available in person in IS Building Room 706
Wednesday: 2pm to 3pm, available virtually at *https://pitt.zoom.us/j/91954241565*
Thursday: 11am to 12pm and 1pm to 2pm, available in person in IS Building Room 706
Friday: 11am to 12pm, available virtually at *https://pitt.zoom.us/j/91954241565*

Announcements

Save the Date:

Professor Daqing He, and the Department of Informatics and Networked Systems (DINS) are pleased to announce that we will be hosting a Celebration Reception for all students graduating from DINS this term. You are more than welcome to bring your family and friends to this casual celebration.

Please join us for two events celebrating Academic Year 2022-2023 graduating students:

School of Computing and Information Spring 2023 Graduate Recognition Ceremony

April 29 | SCI Graduate Recognition Ceremony The Spring 2023 SCI Graduate Recognition Ceremony will be held on-campus from 2 - 4:30 p.m. on the first floor of Lawrence Hall. his will include a formal School-wide ceremony as well as a reception/social hour with light refreshments.
Those who applied to graduate from one or more degree or certificate programs in SCI in Spring 2023 can RSVP here.

Department of Informatics and Networked Systems Reception
Friday, April 28
4:00 p.m.
Information Sciences Building, Room 316
Both undergraduates and graduates of the programs in the Department of Informatics and Networked Systems are welcome. Additional information including RSVP coming soon.

Events

Graduate and Professional Student Appreciation Week

We are always excited to take part in this national initiative calling attention to the contributions, impact and value of graduate and professional students within the campus community. Please join us as we celebrate YOU, your successes, and your many contributions to the University and our community during GPSAW. You can find a full schedule of events here: Graduate and Professional Student Appreciation Week | Graduate Studies (pitt.edu)

Engineering Secure and Privacy-Preserving Systems

Jaideep Vaidya, Distinguished Professor of Computer Information Systems at Rutgers University and the Director of the Rutgers Institute for Data Science, Learning, and Applications

April 12, 2023

11:00 am - 12:00 noon

in-person -- 538-539 Conference Room in 130 North Bellefield Avenue, across the street from the IS Building. Refreshments will be served.

To attend virtually -- https://pitt.zoom.us/j/93846645007

Meeting ID: 938 4664 5007

Abstract: In the current digital age, data is continually being collected by organizations and governments alike. While the goal is to use this data to derive insight and improve services, the ubiquitous collection and analysis of data creates a threat to privacy. Furthermore, the digitization and centralization of data creates attractive targets for cyber criminals,

with security breaches harming both individuals and organizations. In this talk, we discuss the current state of the art in engineering secure and privacy-preserving systems, presenting our recent work on access control configuration and management, synthetic data generation, and privacy-preserving analytics which is crucial to maintaining organizational security and privacy.

Biography: Jaideep Vaidya is a Distinguished Professor of Computer Information Systems at Rutgers University and the Director of the Rutgers Institute for Data Science, Learning, and Applications. He received the B.E. degree in Computer Engineering from the University of Mumbai, the M.S. and Ph.D. degree in Computer Science from Purdue University. His general area of research is in security, privacy, data mining, and data management. He has published over 200 technical papers in peer-reviewed journals and conference proceedings, and has received several best paper awards from the premier conferences in data mining, databases, digital government, security, and informatics. He is an ACM Distinguished Scientist, an IEEE and AAAS Fellow and served as the Editor in Chief of the IEEE Transactions on Dependable and Secure Computing.

Career/Academic Opportunities

ASIC Design Verification Engineer II

Cisco
On-site ·
Maynard, MA

Application deadline
May 5, 2023 12:00 AM
What You'll Do
The ASIC Design Verification Engineer will be a member of a team working on next generation 100G-1T coherent optical communications products. This role is focused on verifying highly-complex ASICs that are used in these next-generation telecom systems. The engineer in this role uses sophisticated verification techniques to complete advanced individual contributions to the projects. There are opportunities to develop process improvements for the team and to coordinate with other engineers within the engineering community to add value to the ASIC projects.

This engineer must be a fast-learning, self-motivated effective person who is able to operate in a fast-paced, dynamic and highly technical environment. A successful candidate will be energetic, collaborative and passionate about learning how to deliver the most advanced high speed optical products in the world. Knowledge of object-oriented verification methodologies is required.
* Develop detailed and comprehensive test plans
* Develop verification test benches
* Timely execution of test plans
* Assist with chip level design tradeoffs by working with design engineers
* Participate in review of design verification coding and coverage metrics
* Participate and assist in FPGA emulation efforts
* Work collaboratively with team to develop & incorporate latest technologies & processes
(41) ASIC Design Verification Engineer II | Cisco | Handshake (joinhandshake.com)

ASIC Hardware Development Engineer Intern, Annapurna Labs

Amazon

On-site ·

Austin, TX

Application deadline

June 16, 2023 3:00 AM

DESCRIPTION

In Annapurna Labs we are at the forefront of hardware co-design not just in Amazon Web Services (AWS) but across the industry. The work we do is cutting-edge and internet-scale while also being deeply important to our customers. We design and build every component of our hardware and software to come together into products that our customers use for accelerated computing: either Machine Learning acceleration, or FPGA acceleration. We get our hands dirty, from creating our own silicon, pushing the electrons in the right direction, ensuring our hardware is functional and healthy, and managing the full lifecycle of our systems at the huge scale and complexity of AWS. If you're interested in ""building a complete product"" from inception to delighted customers, Annapurna is a fantastic choice.

As a member of the Cloud-Scale Machine Learning Acceleration team you'll be responsible for the design and optimization of Software and Hardware in our data centers including technologies such as AWS Inferentia which is a machine learning inference accelerator designed to deliver high performance at low cost.

Key job responsibilities

· Be part of electrical validation team for chip and acceleration cards.

· Work on schematic design for new acceleration cards.

· Support the team lab automation Hardware infrastructure.

· Be involved with AWS Servers testing

· Participate in modeling and simulation of interconnects

BASIC QUALIFICATIONS

· Enrolled in a BS degree program or higher in Electrical Engineering, Computer Engineering, or a related field

· Project/Internship experience with x86 Architecture

· Familiarity with schematic design and layout review of PCBs

· Project/Internship experience with automation

PREFERRED QUALIFICATIONS

· Transmission lines knowledge

· High-speed design

· Knowledge of DC to DC converters

· Familiarity with Linux

· Familiarity with simulation and modeling tools such as Matlab, ADS and field solvers

(41) ASIC Hardware Development Engineer Intern, Annapurna Labs | Amazon | Handshake (joinhandshake.com)

Enrollment Dates

April 7: Last Day for Fall Term Enrollment Appointments

**********Please be advised, that if you have any questions, you can always reach out to me via the email and phone number below. **********

Regards,

James Petraglia (Pa-trail-ya)